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Post-correction of Analog-To-Digital Converter for Different Input signals

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Abstract: ***A novel post correction method with real-time FPGA implementation is proposed to correct the distortion generated by high-speed Analog to Digital Converters (ADCs). It is achieved by simplifying the dynamic deviation reduction based Volterra series to form an accurate model to effectively compensate both static nonlinearities and memory effects. Both post correction model generation and model extraction modules can be readily implemented in FPGA, which provides great flexibilities in realizing real-time calibration. Experimental results demonstrated that excellent calibration performance can be achieved with very low implementation complexity by employing the proposed method. The fundamental observation, upon which this work is motivated, is that practical analog-to-digital converters are prone to produce errors, i.e., deviations from the ideal operation. The term 'post correction' indicates that the correction methods considered in this work are applied after the converter, thus operating on the digital signal provided from the output. One of the constraints for this work is that the internal signals and states of the analog-to-digital converter under consideration are unavailable to us. The goal of the correction is, naturally, to make the corrected output from the converter more true to the ideal output, in some sense; as we will see later on, there are many ways to measure the performance of a converter. Error correction of ADCs has received increasing attention during the last two decades. These methods have in common that the ADC to be corrected is treated as a closed entity, i.e., internal signals and states of the ADC are not available, and the calibration and correction methods must operate outside of the converter. Moreover, the correction is dependent on the output signal x(n) of the ADC to be corrected. That is, the correction is an operation incorporated after the ADC, hence the name post-correction. This paper introduces the present status of analog to digital converter for sine waveform (sine wave). Based on the fundamental principle, the paper then focuses on the different input waveforms such as pulse, triangular type, and square sine for analog to digital converter and compared few ADC parameters like SFDR and SINAD.***

Index Terms: Post correction, SFDR, SINAD, square wave, sine wave.

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I. INTRODUCTION

Analog to Digital Converter (ADC) takes an important role in communication systems and various applications, such as electronic devices, instrumentation and sensor based networks. Implementation of various communication applications in digital domain being the current trend, there is a need for ADC. Industry is benefitted by the Digital implementation in two-fold: first the adaptability of the framework will increase and secondly the cost viability, thus increasing execution of the framework. ADCs are non-linear for high data rate and dynamic range. This causes distortion of the source signal and also the signal mismatch. Hence the system performance degrades to a large extent. With enhancement in CMOS technology, cost-effective low power utilization digital circuit can be produced. This will make the calibration of digital signals popular in ADC calibration. In the present scenario, a significant attention is given to "black-box" based digital post-corrections. The term 'post correction' indicates that the correction methods considered in this work are applied after the conversion, thus operating on the digital signal provided from the output. Error correction of ADCs has received increasing attention during the last two decades. These methods have in common that the ADC to be corrected is treated as a closed entity, i.e., internal signals and states of the ADC are not available, and the calibration and correction methods must operate outside of the converter. Moreover, the correction is dependent on the output signal x(n) of the ADC to be corrected. Both post correction model generation and model extraction modules can be readily implemented in FPGA, which provides great flexibilities in realizing real-time calibration. The model trials led by previous researchers are listed for calibration of post correction. To perform a model extraction algorithm, recursive least-square (RLS) is picked with a fast convergent speed. The author Gong Pu, discussed about correction of errors that occurred inside ADC using Mat lab. But practical implementation is somewhat difficult using Mat lab code. [2] Pradip mane in his publication explained about SFDR and SINAD of ADC's using RLS algorithm. Hassan Hani Slim discussed in his paper about Gain and mismatch errors of ADC's. Shahzad saleem discussed in his work, the ADC errors such as frequency mismatch, gain, and mismatch in timing using FxLMS algorithm. [2-4] Yashar Hesamiafshar elaborated about SFDR and gain mismatch of ADC using DFT technique.

The bandwidth problems of ADC are discussed in the paper "Correction of mismatches in a time interleaved analog to digital converter in TI ADC". In all the works referred, the research was about the parameters of ADC's like SFDR, SINAD, gain, offset etc, by using different algorithms Like RLS, FxLMS, and LMS etc. To measure all the above errors and parameters of ADC, sine wave is taken as input or reference signal. [5,6]

The analog signal may be in any form and it is not mandatory to be in sine. Hence analysis is done for different input signals like pulse square and triangle and the error values of ADC for different type of input signals like pulse, triangular and square etc. This work, "Post-correction of ADC for Diferent Input signals" focus on SFDR values of different input signals like square sine, pulse, and triangular.

$$e_{n-1}(n) = d(n) - y_{n-1}(n) \quad \ldots\ldots.(5)$$

The estimate of past samples of output signal, error signal and filter weight, in the RLS Algorithm requires higher memory requirements [7].

Table 1 demonstrates that, the execution of RLS adaptive algorithm is high as compared to other algorithm due to the less mean-square error (MSE) [7].

Table 1: Performance Comparison of Adaptive Algorithms

S no	Algorithm	MSE	Complexity	Stability
1	LMS	$1.5x10^{-2}$	2N+1	Less stable
2	NLMS	$0x10^{-3}$	3N+1	Stable
3	RLS	$6.2x10^{-3}$	$4N^2$	Highly Stable

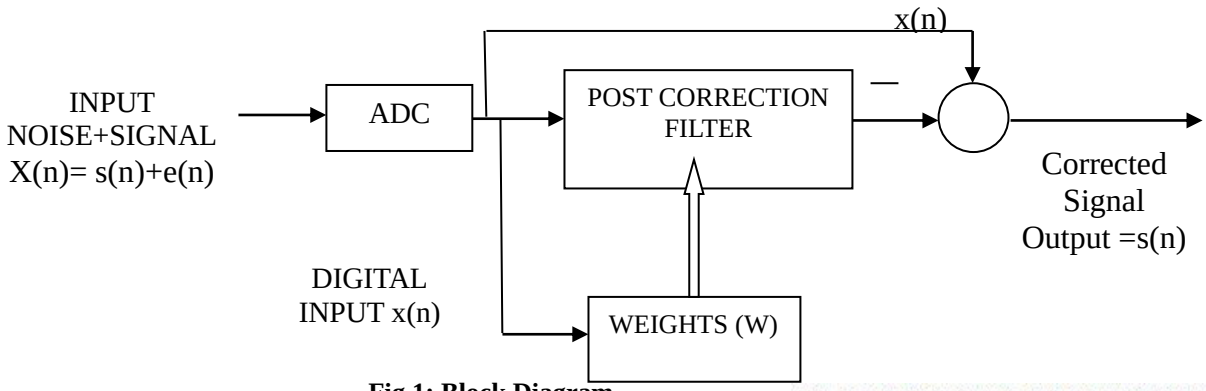

Fig 1: Block Diagram

II. II. IMPLEMENTATION METHODOLOGY:

Second order statistics can't be indicated in many DSP applications such as channel equalization, cancellation of echo and noise. Hence, Adaptive filters implemented with optimizing algorithm are employed in such applications, which adapts on itself the performance based on the input signal. Adaptive algorithm utilizes an individual convergence factor that is refreshed at every emphasis for each adaptive filter coefficient. Recursive Least Square (RLS) algorithm adaptive filter is a calculation which recursively finds the filter channel coefficients that limit a weighted linear least squares cost work identifying with the information signals.

When working in time varying conditions, the excellent performance is the biggest advantage of RLS algorithms, at the expense of an expanded computational multifaceted nature and some stability issues. In this calculation the filter tap weight vector is refreshed utilizing the equation.

$$w(n) = w^T(n-1) + k(n)\, e_{(n-1)}(n) \quad \ldots\ldots. (1)$$

$$k(n) = u(n) / (\lambda + X^T(n)\, u(n)) \quad \ldots\ldots.(2)$$

$$u(n) = w_{\lambda}^{-1}(n-1)\, X(n) \quad \ldots\ldots\ldots(3)$$

Eq. (2) and (3) are intermediate gain vector used to process tap weights. Where λ is a positive constant near to, but less than 1. The filter response is figured utilizing the filter tap weights of above iteration and the current vector input as in Eq. (4) [7] .

$$y_{n-1}(n) = w^T(n-1)\, X(n) \quad \ldots\ldots.(4)$$

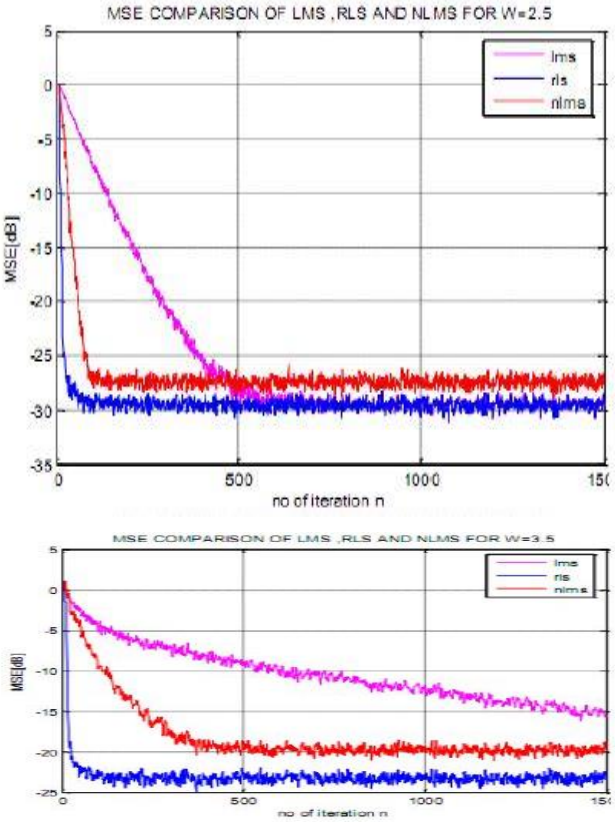

Figure 2: Convergence Comparison for different values of wait (W=2.5, W=3.5)

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III. SIMULATION RESULTS AND OBSERVATION

As per the literature survey, Researchers verified the SFDR for only Sine signals. They have not demonstrated the list of SFDR for different signal shapes like pulse, triangle, and Square. In this article, different signals like pulse, square, sine and Triangle waveforms with noise as input signals are applied to the system the post correction of analog to digital converters and the results are verified.

When a sinusoidal wave is applied as input to the ADC Post-Correction, it is observed that the sine is not corrected immediately. The reason is that, in the code only particular bit numbers are listed to correct up to 15-26 bits after the 26th bit, the wave that is given is not corrected perfectly. The main advantage of RLS algorithm is it will automatically generates the weight codes (coefficients) W (n).It will take previous bits as first input W (0) from Post-Correction Block or from code by considering the first bit remaining coefficients will be generated from the Model extraction or from weight codes generation Block.

Table 2: Different Waveforms Vs SFDRs

S.NO	WAVEFORM NAME	SFDR
1	Sine Signal	94.80Db
2	Triangle Signal	87.88Db
3	Pulse Signal	94.5dB

Table 3: Different Weight Codes VsSFDR Values

S.NO	WEIGHT CODES	SFDR VALUES (dB)
1	4	75.45 dB
2	8	87.88 dB
3	16	94.80 dB
4	32	95.89 dB
5	64	98.66 dB

IV. SIMULATION RESULTS

Figure: 3 describes the adding of noise to sine wave had given ADC and figure 6-7 post correction of ADC for noise added sine wave.For sine wave Post correction is giving 100% corrected signal.

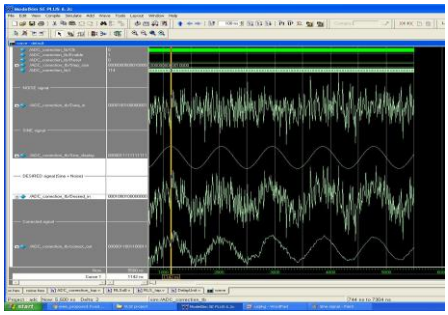


Figure 3: Post-Correction output for SINE Waveform Input

Figure: 4 describes the adding of noise to sine+triangle wave had given ADC and figure 13 is digital post correction of ADC for noise added sine+trianle wave. For sine+Triangle wave Post correction is giving 84% corrected signal .

Figure: 5(a) describes the adding of noise to sine+square wave had given ADC and figure 5(b) is digital post correction of ADC for noise added sine+square wave. For sine+Square wave Post correction is giving 84% corrected signal.

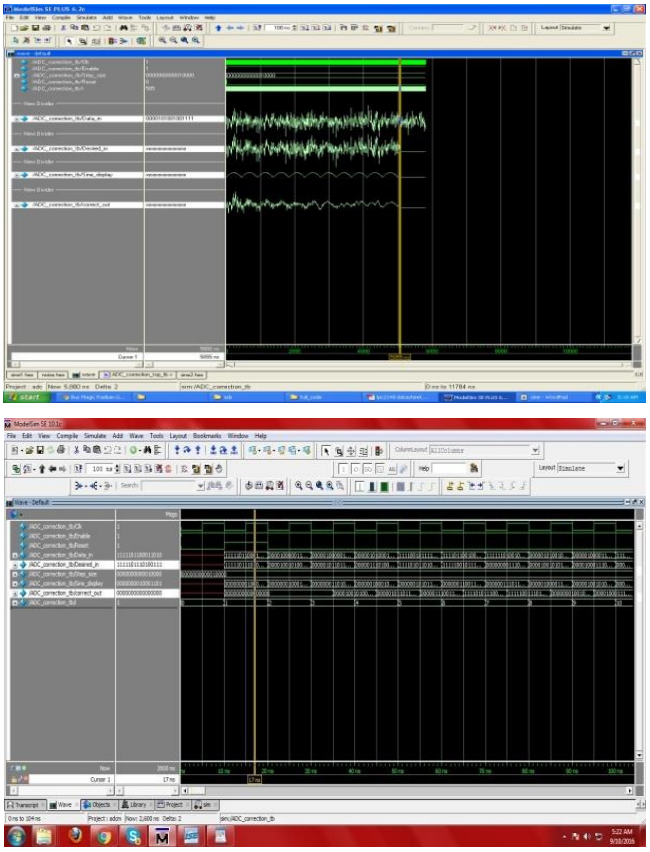
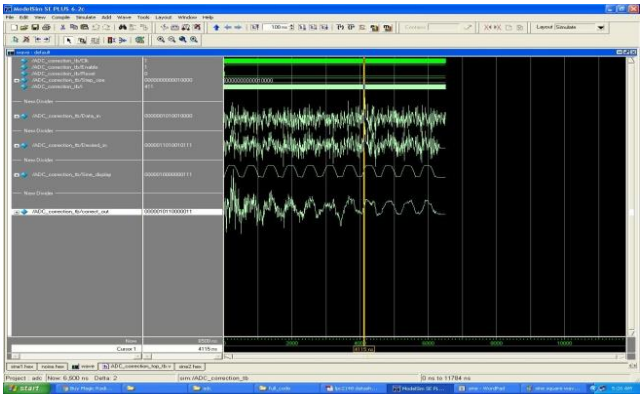


Figure 4 :Output of ADC Post-Correction for (a) Triangle (Sine+Triangle) like Signal (b) Triangle Signal in Binary



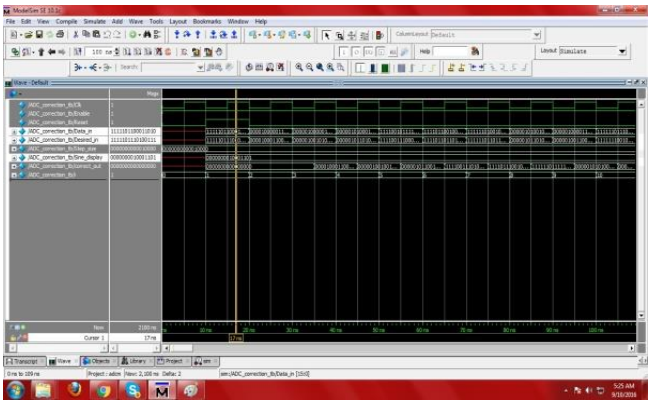


Figure 5: Output of ADC Post-Correction for (a) Square (Sine Square) like Signal (b) Square Signal in Binary

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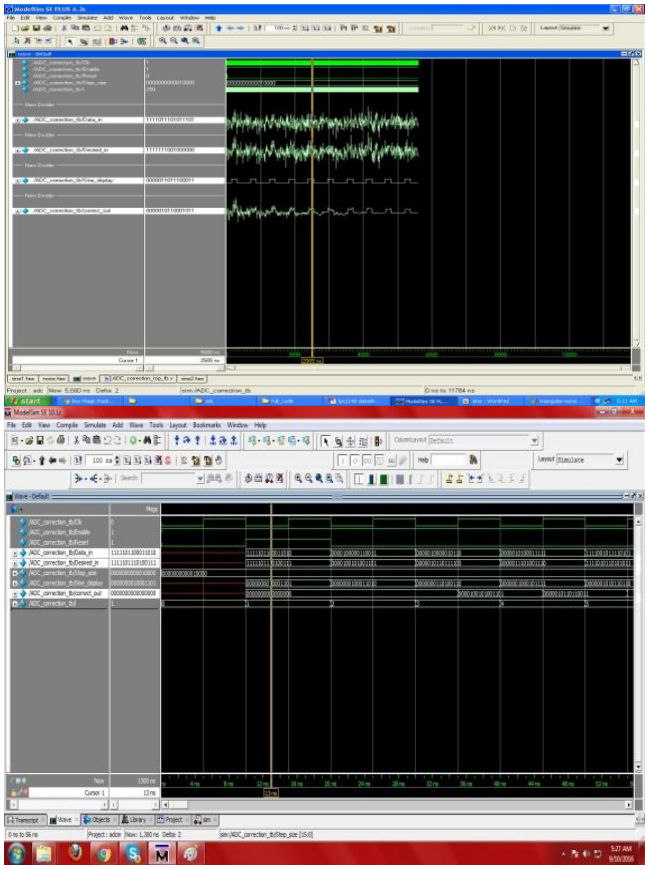

Figure 6: Output of ADC Post-Correction for (a) Square Signal (b) Square Signal in Binary

Figure: 6(a) describes the adding of noise to square wave had given to ADC and figure 6(b) describes about the binary values of Square wave samples and how accurately it retrieving the digital data from noise added data to pulse wave.For Square wave Post correction is giving 94% corrected signal.

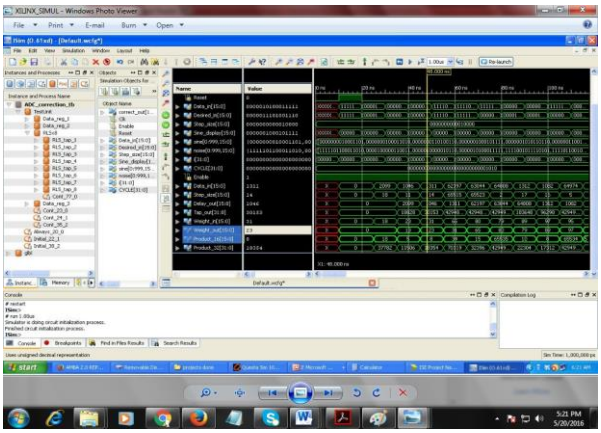

Figure 7: Weight Calculation Data in Hexadecimal for Post-Correction

Figure: 7 describes about the hexadecimal values of sine wave samples and how accurately it retrieving the digital data from noise added data to sine wave. Figure: 8-9 describes the adding of noise to Pulse wave had given to ADC and figure 10 post correction of ADC for noise added Pulse wave. For Pulse wave Post correction is giving 100% corrected signal.

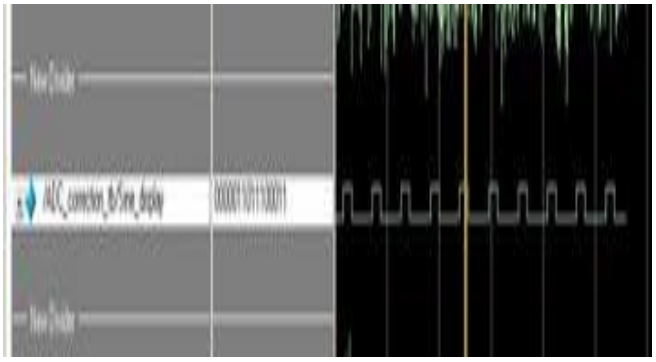

Figure 8: Input Pulse Waveform of ADC

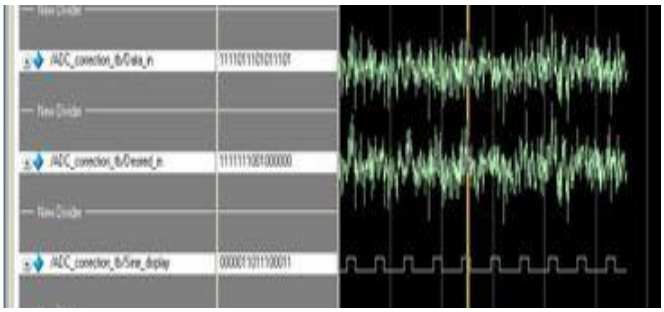

Figure 9: Input Waveforms Pulse+Noise of ADC

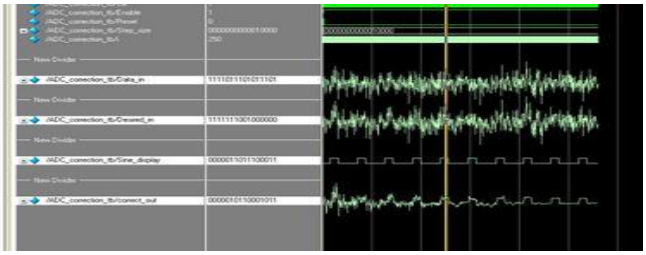

Figure 10: Output Waveform of ADC Post-Correction for Pulse

V. CONCLUSION

Post correction approach is proposed to compensate for the nonlinearities of the ADCs including both static nonlinearities and memory effects. Different from previously reported ADC post correction solutions, the entire calibration system has been implemented in digital hardware and can be operated in real time. SFDR measurement of 94.80 db proves the feasibility of this hardware design. The post correction block can be made as a stand-alone module or an add-on element to linearize different sorts of ADCs which is extremely alluring for future incorporated digital circuit design. For sine + square wave post correction and sine + triangle wave Post correction, 84% corrected signal is obtained and square wave post correction is giving 94% corrected signal. 100% corrected signal is obtained with sine wave post correction. By increasing the weight blocks, SFDR will increase and hence performance can be boosted. This proposed model can be implemented in medical applications, communication systems and Mobile applications.

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